A patterning strategy for large area arrays of high density nanostructures

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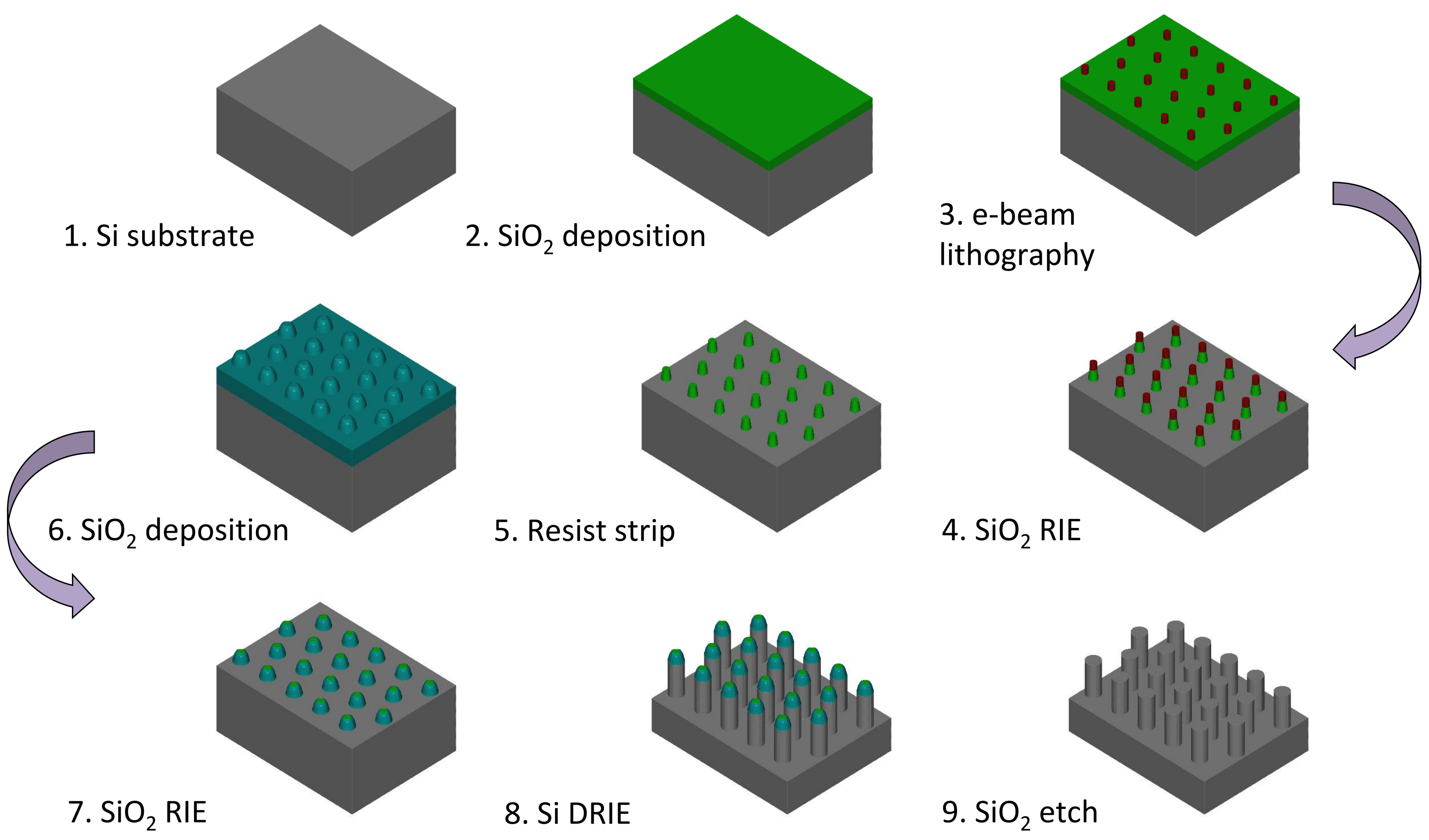
Introduction

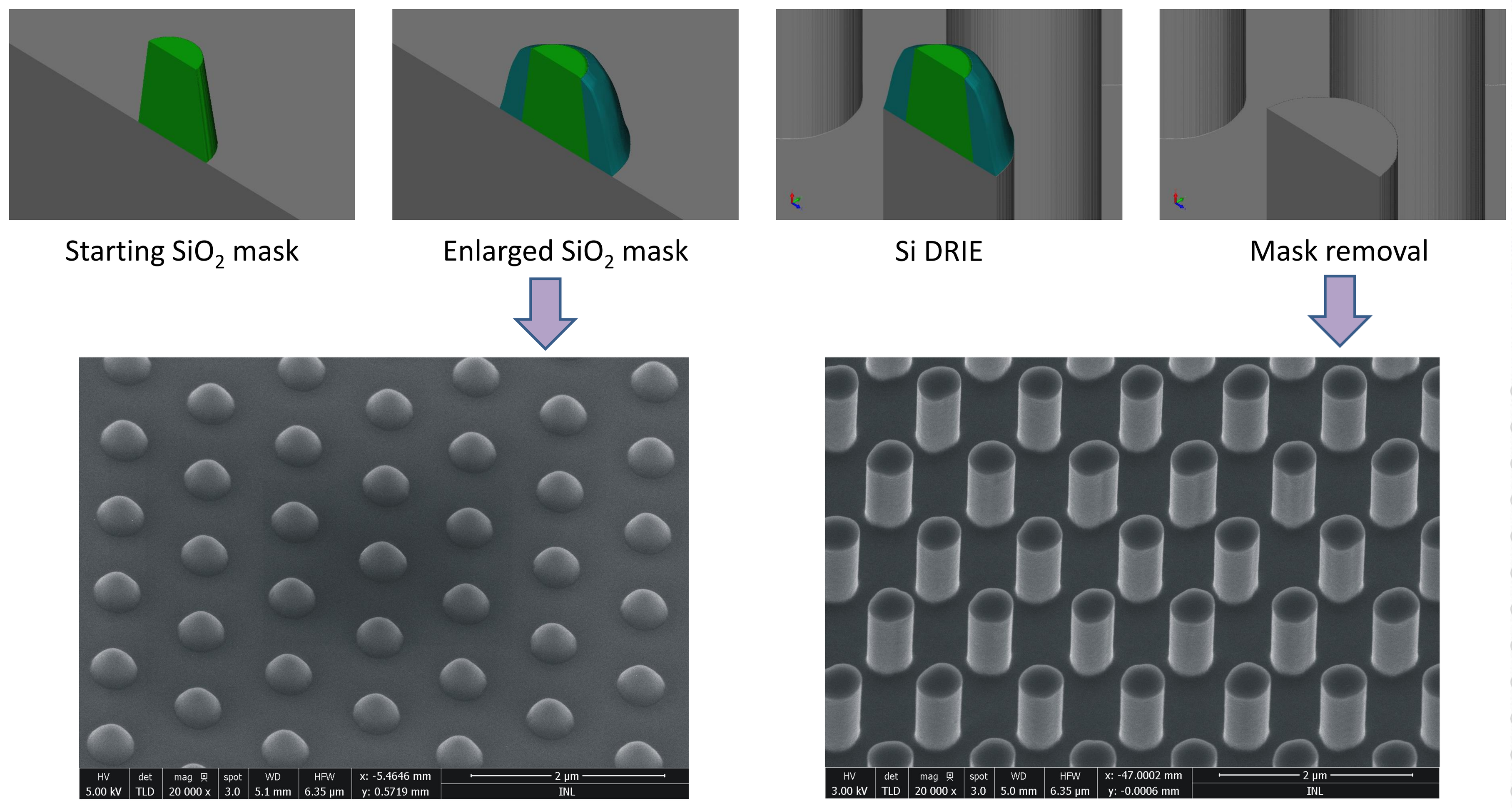
A production-worthy method to implement high density arrays of sub-micron nanostructures at a wafer scale is proposed. It is based on a co-optimization of the layout design, the e-beam lithography exposure and the intermediate SiO_2 hard mask used for the final silicon etch process. The great complexity of the e-beam lithography exposure required at this scale to directly obtain the desired geometries has been reduced by introducing an intermediate hard mask to get independent control of some of the pattern parameters through the fabrication process [1]. Rather than using e-beam lithography to create a resist mask for the etch process, which results in unaffordable exposure times for complex geometries (large patterns of curved structures), a simplified e-beam lithography step has been developed to attain a primary resist mask with needed shape and periodicity, but smaller size.

Experimental Procedure

The e-beam exposure time is minimized through layout design (single shape square approximation) and proper selection of resist exposure conditions. E-beam resist pattern is transferred to the primary SiO_2 hard mask by RIE. After resist removal, the feature size on the final hard mask is fine-tuned using a second SiO_2 deposition and etch-back process that allows the precise growth of the features achieved on the primary hard mask.

Fabrication Process Sequence:



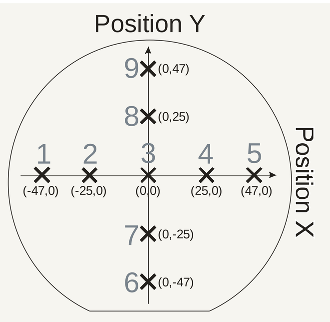


Results and Discussion

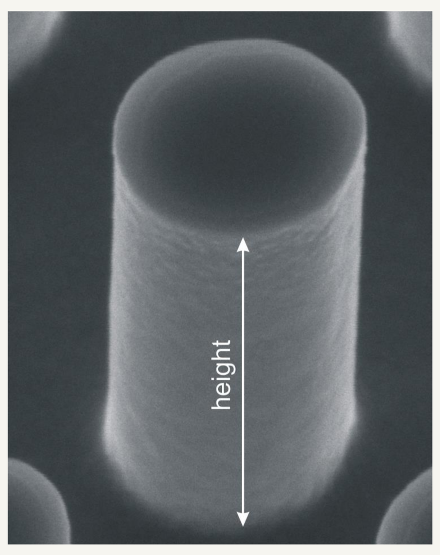
6-inch wafers with circular areas (Ø= 110 mm) covered with regular arrays of Si nanopillars were generated with proposed method. Arrays with 1 μm height circular pillars with Ø= 500 nm distributed in an hexagonal lattice with 1 μm pitch were used for validation.

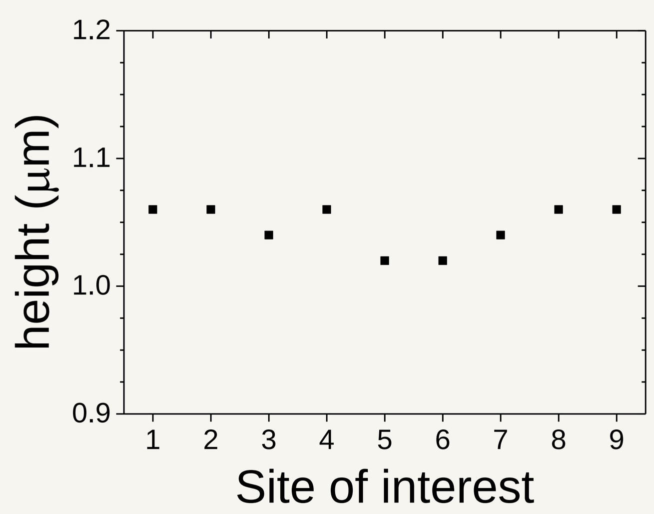
Pattern quality monitoring:

9 sites studied throughout fabrication process.

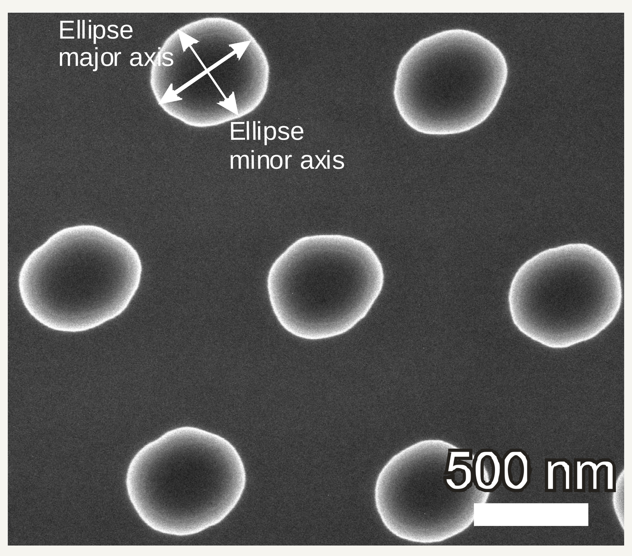


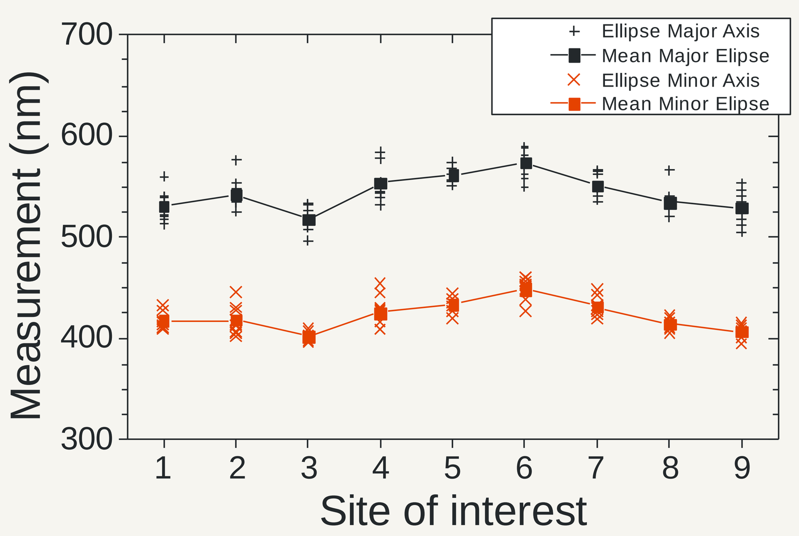
Height of pillars:





Ellipse major and minor axis of pillars:

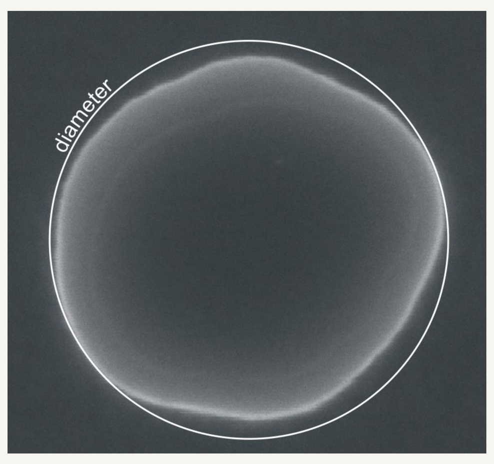


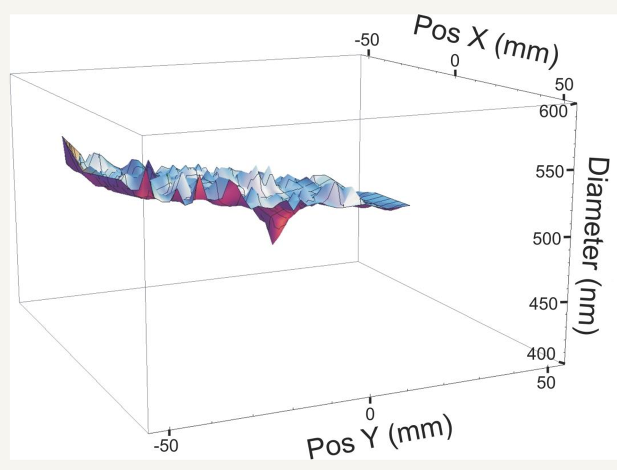


Automated pattern evaluation:

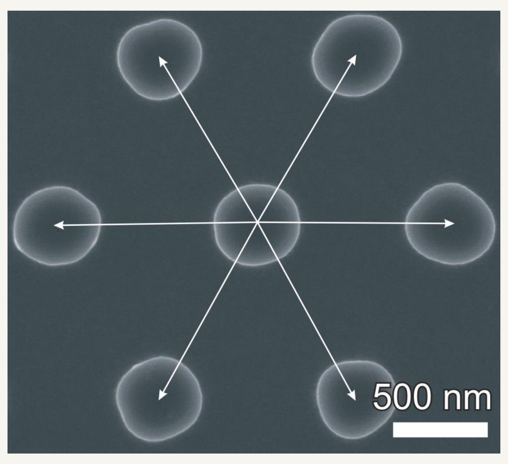
Achieved with image processing routines specially developed to process more than 1000 SEM images obtained with IFast scripting software (on a NanoSEM tool from FEI) in locations covering the full wafer.

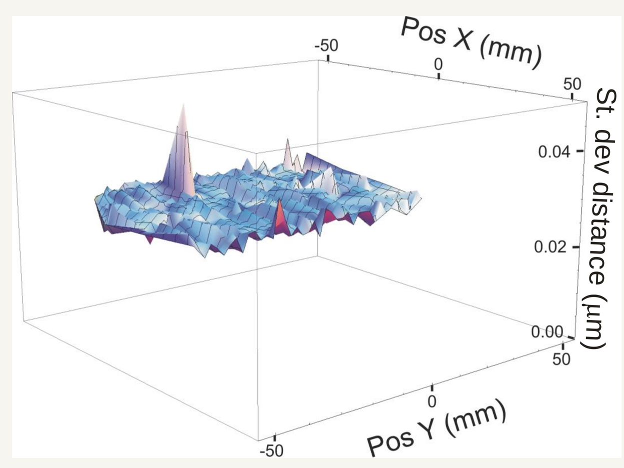
Diameter of the pillars:





Average distance to closest neighbours:





Conclusions

- Height, diameter and periodicity of large nanostructure arrays fabricated at wafer scale with the proposed method have been analysed.
- Large amounts of nanostructures (~ $2\cdot10^8$ pillars), 1% out of ~ 10^{10} pillars on each wafer, have been analysed using a set of automated routines developed for image acquisition and processing.
- Values measured across the wafer show limited variability, with 520 ± 12 nm for pillar diameter, and 1.038 ± 0.03 mm for lattice period.

References

1. Bao, X.-Q., Petrovykh, D. Y., Alpuim, P., Stroppa, D. G., Guldris, N., Fonseca, H., Costa, M., Gaspar, J., Jin, C. & Liu, L. Amorphous oxygen-rich molybdenum oxysulfide Decorated p-type silicon microwire Arrays for efficient photoelectrochemical water reduction. Nano Energy 16, 130142 (2015).

Acknowledgments

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